**CS 223 Fall 2016 Lab Projects**

1 - The project will be done in groups of 2 students. Choose a partner from your section. If a project partner leaves the course for some reason (serious illness, W grade, gives up, etc.) after *November 21,2016*, the other student must continue without him/her and complete the project alone.

2 - The contents of the project will be decided by each group, with these restrictions:

(i) The project should use the BASYS3 board and at least one of the modules on the CS223 Beti experiment board or an equivalent off-board module doing essentially the same thing.

(ii) The project should have a System Verilog HDL component, implemented on the FPGA.

(iii) The project must contain a control section and a data processing section (based on the controller + datapath model of our course).

(iv) Projects should not be copies of existing projects. Pre-written codes may be used in the project if you are adding a significant amount of extra work. If such code (from a book, Internet, or wherever) is used, it should be referenced in your project.

3 - Ideas for projects can come from your or your partner’s imagination, family and friends, news items, YouTube, the Internet, books, magazines, etc. Things that interest you (such as games, or information processing, or music) can be topics. Inputs can be sensors (microphones, fingerprint readers, motion detectors, etc), keyboard, keypad, mouse, buttons/switches, even pre-stored data from memory. Outputs can be motors, display devices, speakers, actuators, etc. Let your imagination soar!

4 - Your project may involve more than the BASYS3 board and the CS223 Beti experiment board. You may use additional chips (A/D, D/A, memory, interface, drivers, etc), additional boards (other FPGA cards, another CS223 Beti board, the CS224 Beti board, etc) and any peripheral devices for input and output that you want. Lots of interesting things are available in the electronics stores of Kizilay and Ulus and on the internet!

5 - Each group should prepare a short Project Proposal, at most two A4 pages, following the specifications given below. To receive full credit, it must be uploaded to the Unilica Assignment before *October 31, 2016.* No proposal will be accepted after *November 7, 2016.*

6 - Each group will submit a short Progress Report to Unilica Assignment, due November 28, *2016*. The report should include an outline of the progress so far. It should also outline the work to be done in the future. It should include the original project proposal and any changes that you have made to it. Details about this report are found in the section below called Progress Report.

7 - The projects should be completed and a Final Project Report describing the project and its implementation should be uploaded to Unilica by the deadline on *December 26, 2016*. The report will contain the design and its implementation, as detailed below in the section about Final Project Report. Your group should also print out a copy of the Final Project Report to submit, and bring it with you to your Project Demo.

8-Each group must upload their Final Project Report , including the System Verilog code in an Appendix as specified below (and any other code used in the project). This report should be a .docx or .pdf file, uploaded to the Unilica Assignment. Name the file *YourProjectName* and include all the code in it. This upload must take place by the deadline on *May 4th, 2016.*

9 - Groups will demonstrate their projects to the instructor and the TA’s in a specially scheduled Demo time, after the last day of the semester. At this demo, both students will explain and present their project, and answer questions, to determine how much of the project each partner has done and/or understands, and how much of the project is working as planned, and how much the project has achieved according to the original proposal. Students will be expected to show their projects during this special Demo time. Students not attending the Demo time will receive 0 points from both the Report and Demo and the Peer Grading. The project will receive a Report and Demo Grade, based on the 4 factors listed below. In addition, each student will give a Peer Grade to the other group member.

10 - Grading will be as follows:

(i) Project Proposal (25%): Clarity and quality of the Project Proposal document, and originality of the idea are the determinants of the grade.

(ii) Progress Report (25%): Clarity and quality of the Progress Report document, the content of the report, and the amount of progress made will determine the grade.

(iii) Final Project Report and Demo (40%): determined as follows:

* Difficulty level (10%) of the project
* Completeness (10%) according to the proposal
* Quality (10%) of the overall design and implementation
* Clarity and quality of the Final Project Report document and the Demo (together, 10%)

(iv) Peer Grading (10%): Group members will give peer grades to each other (from 0 to 10)

Project Proposal

The Project proposal should be at most 2 pages (not counting the cover page). You should upload a file named Partner1Name\_Partner2Name\_ProjectName.docx (or .pdf). It should contain the following 4 sections, each clearly delineated from the others:

1- A cover page with

1. university name, department name, course code# and course name at the top
2. Project Name in the upper middle in large letters
3. names and ID #s and Section #s of the group members in the lower middle
4. date of the report submission at the bottom
5. Description of the project: what is it, what will it do, specify the inputs, outputs and their relationship
6. Equipment to be used: which FPGA board(s), which Beti experiment boards and which I/O modules on the Beti experiement boards, which additional chips, which additional external I/O devices, etc. If extra components are needed and not available in the lab, students should buy them from electronics stores.
7. The deliverables of the Project: Make a table listing everything that will you submit or show during the entire course of the project, and the due date of that Deliverable. This table should include all deliverables even those on the Demo day. You should list all the reports, System Verilog code, the oral presentation of your project, Peer Grading form, etc

**Name of Deliverable Date of Delivery**

|  |  |
| --- | --- |
| Project Proposal report | October 31, 2016 |
| .Project Progress Report | November 28,2016 |
| Project Finai Report | December 26, 2016 |
| ... | ... |

Progress Report

The Progress Report be in a file named Partner1Name\_Partner2Name\_ProjectName.docx (or .pdf) It should contain the following 6 sections, each clearly delineated from the others:

1- A cover page with

1. university name, department name, course code# and course name at the top
2. Project Name in the upper middle in large letters
3. names and ID #s and Section #s of the group members in the lower middle
4. date of the report submission at the bottom

2- A block diagram of the project, showing the top level design. All inputs to and outputs

from all blocks should be named, and identified as specifically as possible. All blocks

should have a name.

3- For each block, give a description of its function. Tell how it will be realized (for

example: “coded in Verilog, implemented on the BASYS3 board’s FPGA chip”, or “HX345

part, purchased from Kizilay”, “coded in C, implemented on an Arduino microprocessor,

etc). If the block is code, tell where the code will be [or has been] obtained from (for

example: “we will write this code”, or “we got this code from the engineer Elif

Yardimsever at Beti”, or “we found this code on the internet at <http://blah.blah/codesafe/>

and will translate it from VHDL to System Verilog”, etc)

4- In a table like the one shown below (*but with your block names!*), list all the blocks and

all the tasks for each block that have been done so far, and which still need to be done.

Make the table as big as you need, and write as much as you can in each box.

**Block name Tasks which have been done Tasks which still need to be done**

|  |  |  |
| --- | --- | --- |
| Input modulator |  |  |
| FIR filters |  |  |
| Sound enhancement |  |  |
| D-to-A converter |  |  |

1. Include your Project Proposal as you submitted it (if you had to submit more than once,

then the one that was accepted in the end). Just copy-paste it into the Progress Report as-is.

6- Write a short list of items in your project *currently* that are different from what you pro-

posed in the Project Proposal. If you currently doing, or planning to do, things differently from what you originally proposed, make clear what those changes are!

Final Project Report

The Final Project Report must contain the following 5 sections, each clearly delineated from the others. Upload it in a file named Partner1Name\_Partner2Name\_ProjectName.docx (or .pdf).

1- A cover page with

1. university name, department name, course code# and course name at the top
2. Project Name in the upper middle in large letters
3. names and ID #s and Section #s of the group members in the lower middle
4. date of the report submission at the bottom

2- A block diagram of the project, showing the top level design of the system. All parts of the system should be represented in the block diagram. All blocks should have a name. All inputs to and outputs from all blocks should be named, the number of bits clearly marked and identified as specifically as possible.

3- For each block in the top-level block diagram, have a sub-section that gives the following:

1. the function of the block—in a sentence, what does the block do?
2. the timing of the block’s inputs and outputs—what timing constraints (if any) are there, regarding frequency, delay, rate of data input/output, delay, etc
3. the description of the block—in a paragraph, how does it do its function?

4- References:

a. for each portion of code in your project that was used directly from another source--identify where that code is used (in which block, in what portion of that block), and state the source of the code.

b. for each portion of code in your project that was modified or translated from another source-- identify where that code is used (in which block, in what portion of that block), and state the source of the code.

c. for each piece of hardware that you obtained from outside Bilkent-- identify where that hardware is used (in which block, in what portion of that block), and tell where you obtained it from, and its cost.

5- Appendices:

1. For each block in your system, the actual design implementation (i.e. the code or circuits that implement it). Code listings should be well-labeled, organized and readable. Circuit diagrams should also be clear and understandable.
2. For any hardware parts you used, the data sheets of those parts.